REMARKS

Two sheets of drawings, which include Figs. 1 and 5 with the corrections approved in the last Office Action, are submitted with this paper.

Minor amendments are made to the specification to correct a misspelling that arose out of the translation of this application from the Japanese language. Specifically, "halls" is corrected to read "holes" in three locations. Applicant submits that the proper reading would have been readily apparent to one of ordinary skill in the art, and that no new matter is added with this amendment. A similar amendment is made to claim 4. Claim 4 is also amended to correct "easing" to "erasing," another readily apparent misspelling.

The application was filed with eighteen claims. Claims 1-6 were elected for prosecution in response to a previous restriction requirement, and claims 7-18 were canceled as being directed to a non-elected invention. Claim 2 was amended in a prior amendment. Claims 1, 3, and 5 are canceled, claims 2, 4, and 6 are amended, and new claims 19-24 are added in this paper. Claims 2, 4, 6, and 19-24 are thus now pending for examination. Examination and allowance of those claims is respectfully requested.

New independent claim 19 is directed to a non-volatile semiconductor memory in which:

> an overlap of [a] drain region with [a] floating gate is larger than an overlap of [a] source region with said floating gate
>
> - and –
>
> a junction depth of said source region is larger than a junction depth of said drain region.

Applicant concedes that the Lu reference describes a memory cell in which "an overlap of [a] drain region with [a] floating gate is larger than an overlap of [a] source region with said floating gate."

The Examiner concedes, though, that the Lu reference *does not* describe that the "junction depth of said source region is larger than a junction depth of said

drain region." *Office Action* mailed May 6, 2002, ¶ 7 (discussing claim 5, now canceled from the application.) The Examiner alleges that:

> it would have been obvious to a person of ordinary skill in the art at the time of the invention to have the source junction depth larger than the drain junction depth as taught by Kume et al. in the device of Lu et al. to make it possible to apply a high erase voltage.

Id.

In fact, though, the Kume reference *does not* clearly teach a device having a source junction depth greater than a drain junction depth. Even if it did, moreover, it does not teach that such a configuration makes it possible to apply a high erase voltage, and one of ordinary skill in the art would not have been led by Kume to incorporate such a feature into the device of Lu.

Kume does not clearly describe a device in which a source junction depth is larger than a drain junction depth. Figure 1 might be supposed to depict such a device, but a closer study of Kume indicates that this is mere imprecision in the illustration of Fig. 1.

Kume's Fig. 1 shows "a flash-erase EEPROM cell with an asymmetric source and drain structure."

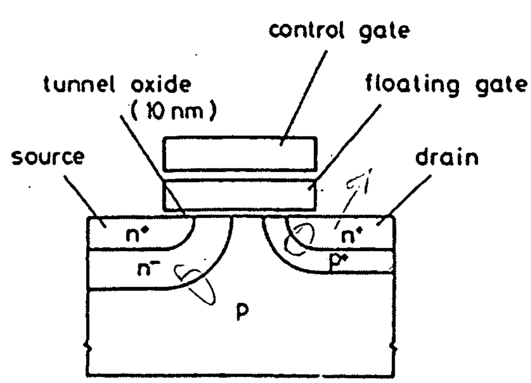

Fig. 1 Cross section of flash-erase EEPROM cell with an asymmetric source and drain structure.

Figure 1 does appear to illustrate a configuration in which the source depth (at the left side of the drawing) is greater than the drain depth (at the right).

The exact dimensions of the memory cell, though, are specified in Table 1, which is printed at the bottom left of the same page.

Table 1 Feature sizes of memory cell

Process	Double Polysilicon Technology	
Gate Length		1.2 μm
Gate Width		1.0 μm
Gate Oxide Thickness		10 nm
Inter-poly Oxide Thickness		25 nm
Diffusion Depth	n^+	0.3 μm
	n^-	0.5 μm
	p^+	0.5 μm
Cell size		2.9 x 3.2 μm^2

The source junction depth is equal to the sum of the diffusion depths of the n^+ and n— regions (0.3 μm + 0.5 μm = 0.8 μm). The drain junction depth is equal to the sum of the diffusion depths of the n^+ and the p^+ regions (0.3 μm + 0.5 μm = 0.8 μm). Notwithstanding any imprecision in the sketch Kume's Fig. 1, the source junction depth is *not greater* than the drain junction depth, as new independent claim 19 requires. In Kume, the source junction depth and drain junction depth are both 0.8 μm. The cited art thus fails to teach every limitation of new independent claim 19, and that claim is therefore allowable over that art.

Even if one were to accept the apparent differential in the sketch of Fig. 1 over the precise dimensions set out in Table 1, there would still be no motivation for one of ordinary skill in the art to modify Lu to include *a source junction deeper than a corresponding drain junction* for the purpose of applying a higher erase voltage.

Kume teaches that its "asymmetric structure" for the source and drain regions allows high voltage erase operations. This "asymmetry," though, does not involve a difference in the depths of the two regions. Kume's asymmetry lies instead in the different compositions of the source and the drain.

The Kume reference teaches the following, on its first page, in the right hand column:

> In order to achieve high speed operation for both programming and erasing, an asymmetric structure has been adopted in the source and drain regions.
>
> The source region has an n^+–n^- double diffused profile, which makes it possible to apply a high voltage to the source for erase operation. A p^+ shield region surrounding the drain junction suppresses an undesirable punchthrough current during erasing, even in a submicron gate length. This structure also improves programming efficiency.

Kume then goes on to discuss the preferred doping level for the n^+ region.

Kume does not suggest that a difference in source and drain region depths provides better erase characteristics. Nor does Kume describe any "asymmetry" in those depths. Kume's asymmetry is in the different compositions of those two regions (n^+–n^- in the source *vs.* n^+– p^+ in the drain).

If, therefore, one of ordinary skill in the art were looking to Kume's reference for a suggestion for improving the performance of Lu's device, that person would have been led to incorporate an "asymmetric" configuration in which the source and the drain had different material compositions. That person of ordinary skill would not have been led to use a configuration with a source and a drain having different depths. Kume does not teach or describe such a configuration (*see* Kume's Table 1 and the discussion above), and to the extent Kume's Fig. 1 might suggest such a configuration, Kume does not teach it as an effective way to improve the performance of Lu's memory cell.

New independent claim 19 is thus allowable over the Examiner's proposed combination of Lu with Kume, either because those references fail to teach every element of the claim, or in the alternative because their is nothing in either reference that would have motivated one of ordinary skill to make the combination the Examiner suggests. The allowance of claim 19 is therefore respectfully

requested, along with dependent claims 2, 4, 6, and 20, each of which depends from claim 19.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is invited to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6711 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

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Version with markings to show changes made:

IN THE SPECIFICATION:

Please replace the paragraph at page 4, line 34 – page 5, line 3, with the following amended text:

> Further, in the case of the memory cell wherein the electric charge accumulating layer receiving the implantation of the hot electrons is defined as the trap level within the insulating layer, the erasing operation may involve pulling the electrons held by the trap level to the drain region by tunneling, or more preferably may involve neutralization of the electrons held by the trap level by injecting [halls] holes generated in the vicinity of the drain region.

Please replace the paragraph at page 13, lines 16-29, with the following amended text:

> On the other hand, the erasing operation is that an electric field is applied to between, e.g., the drain region 9 and the control gate 6, and the electrons trapped by the interface level within the insulating layer 20 are pulled to the drain region 9. Alternatively, considering that the electrons can not easily be released only by the electric field, an electron accumulated state is neutralized by injecting [halls] holes. To be specific, the source region 8 is grounded, the control gate 6 is given a negative potential, and the drain region 9 is given a positive high potential, respectively. Band-to-band tunneling is thereby induced by the drain junction, and the generated [halls] holes are injected into the insulating layer 20. with this operation, the erasing

efficiency becomes by far higher than in the case of releasing the electrons by the electric field.

IN THE CLAIMS:

2. (Twice Amended) The non-volatile semiconductor memory according to claim [1] 19, wherein an impurity dose quantity of said source region is larger than an impurity dose quantity of said drain region.

4. (Amended) The non-volatile semiconductor according to claim [1] 19, [wherein said] and further comprising an electric charge accumulating portion [is] in an insulating layer having a trap level therein, said insulating layer being provided between said channel region and said control gate[, and];

wherein an [the easing] erasing operation involves neutralization of [the] electrons held by the trap level by injecting [halls] holes generated in the vicinity of said drain region.

6. (Amended) The non-volatile semiconductor according to claim [1] 20, wherein said side wall [is composed of] comprises a first side wall and a second side wall formed on the first side wall, and wherein said drain region is formed in self-alignment with said first sidewall and said source region is formed in self-alignment with said second side wall.